CHIP DEBUGGING USING INCREMENTAL RECOMPILATION AND REGISTER INSERTION

ABSTRACT OF THE DISCLOSURE

While debugging, a user chooses an incremental recompile. Internal signals of interest and output pins are selected, and a number of additional registers are chosen to insert in the path of each internal signal. A clock is selected for the registers. An incremental recompile of the compiled design compiles a routing from each internal signal to an output pin via the added registers. The database building and logic synthesis stages are skipped. The post-fitting logical netlist and routing netlist are retrieved. The new registers are created and the internal signal is connected to the output pin atom in the logical netlist. The fitter places and routes the connections to create a new routing netlist and then the new routing netlist is output into a programming output file (POF) in a form suitable for programming the PLD. The original routing netlist is undisturbed. The user views the internal signals at the output pins chosen. The user may iterate through this process many times in order to debug the PLD. The debugging assignments may be deleted.